CLAIMS:

1. (Currently amended) A pulse width limiting ~~circuit~~ system, comprising:

a clock signal correction block configured to receive a conditioned clock ~~pulse~~ signal and generate a corrected clock output signal, wherein the clock signal comprises a train of clock pulses, each of which has a rising clock edge, a falling clock edge and a variable width;

a block delay module, coupled to the clock signal correction block, configured to accept an unconditioned clock signal and introduce a specified pulse width delay to thereby generate the conditioned clock signal, wherein the block delay module comprises a plurality of delay sub-blocks of fixed delay; and

a high low clock pulse shuttle circuit, coupled to the clock signal correction block, configured to accept the conditioned clock signal ~~output~~, wherein the high low clock pulse shuttle comprises a first field effect transistor (FET) coupled to the correction block and a second FET coupled to a conditioned clock signal output interconnect, and wherein individual delay sub-blocks of the plurality of delay sub-blocks of the block delay module are disconnected and reset based on the unconditioned clock signal.

2. (Currently amended) The system of claim 1, wherein the unconditioned clock ~~input~~ signal is ~~coupled~~ input to the source of a ~~positive~~ P-type FET in the high low clock pulse shuttle.

3. (Currently amended) The system of claim 1, ~~where a correction block circuit~~ wherein the system further comprises ~~a correction unit and~~ a leak detector unit coupled to the clock signal correction block, wherein the clock signal correction block is employed to transmit the conditioned clock ~~pulse~~ signal to the high low clock pulse shuttle.

4. (Currently amended) The system of claim 2, wherein the high low clock pulse shuttle is coupled to an interconnect, wherein the interconnect is employed to convey ~~an unmodified~~ the unconditioned clock ~~pulse~~ signal.

5. (Currently amended) The system of claim 1, further comprising a node to transmit [[the]] a clock pulse of the unconditioned clock signal between stages of a delay sub-block.

6. (Currently amended) The system of claim 1, further comprising a node to transmit the conditioned clock ~~pulse~~ signal between [[the]] a last delay sub-block of the plurality of delay sub-blocks and the clock signal correction block.

7. (Currently amended) The system of claim 1, further comprising a node to transmit the conditioned clock ~~pulse~~ signal between the clock signal correction block, the high low clock pulse shuttle circuit and a clock pulse inverter.

8. (Original) The system of claim 3, further comprising a leak detector calculating a voltage potential between two digital devices.

9. (Currently amended) The system of claim 7, wherein an uncorrected clock pulse bypasses the clock signal correction block and the high low clock pulse shuttle circuit for delivery through the clock pulse ~~output~~ inverter.

10. (Original) A method for performing a plurality of clock pulse widths limiting in clock pulses, comprising:

initiating a clock in pulse as a result of a clock cycle;
routing a clock pulse;
initiating a correction block;
determining a voltage leak;
forwarding a clock pulse through a clock shuttle node;
injecting a clock pulse through a block delay module;
sequentially advancing a clock pulse through delay sub-blocks;
disconnecting and resetting individual delay sub-blocks;
altering a clock pulse that is greater than a predetermined pulse width; and

substantially passing through a clock pulse less than or equal to a predetermined pulse width.

11. (Currently amended) The method of claim [[11]] 10, wherein a clock pulse width is selected for correction by a specific state within a correction block.

12. (Original) The method of claim 11, wherein a clock pulse width is deselected for correction by a specific state within a correction block.

13. (Original) The method of claim 11, wherein a selected clock pulse is passed through a clock pulse correction block and checked by a leak detector.

14. (Original) The method of claim 11, wherein a deselected clock pulse is passed through a clock shuttle and output through a clock pulse inverter.

15. (Original) The method of claim 11, wherein a selected clock pulse is passed through a clock pulse correction block, checked by a leak detector, and input to a block delay module.

16. (Original) The method of claim 11, wherein the block delay module is conditioning the clock pulse using a series of delay sub-blocks.

17. (Original) The method of claim 11, wherein the delay sub-blocks are sequentially disconnecting and resetting as the clock pulse is passing.

18. (Original) The method of claim 11, wherein the conditioned clock pulse is output to the correction block.

19. (Original) The method of claim 11, wherein a completely conditioned clock pulse outputs to a conditioned clock pulse dependent device.

20-21. (Canceled)

22. (New) A method of providing a pulse width limiting circuit, comprising:

providing a clock signal correction block configured to receive a conditioned clock signal and generate a corrected clock output signal; and

providing a block delay module, coupled to the clock signal correction block, configured to accept an unconditioned clock signal and introduce a specified pulse width delay to thereby generate the conditioned clock signal, wherein the block delay module comprises a plurality of delay sub-blocks of fixed delay, and wherein individual delay sub-blocks of the plurality of delay sub-blocks of the block delay module are disconnected and reset based on the unconditioned clock signal.

23. (New) A pulse width limiting circuit, comprising:

a correction block circuit; and

a block delay module coupled to the correction block circuit, wherein the block delay module comprises a plurality of delay sub-blocks, and wherein:

individual delay sub-blocks are disconnected and reset based on an input clock,

a clock pulse is sequentially advanced through the plurality of delay sub-blocks such that the clock pulse is altered by the delay sub-blocks if the clock pulse has a pulse width greater than a predetermined pulse width, and

the clock pulse is substantially passed through the pulse width limiting circuit if the pulse width of the clock pulse is less than or equal to the predetermined pulse width.